



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,006	10/21/2003	Robert M. Steinhoff	TI-35703	4784
23494	7590	01/23/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			ARENA, ANDREW OWENS	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/690,006

Applicant(s)

STEINHOFF ET AL.

Examiner

Andrew O. Arena

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-20 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Clukey (US 5,644,460), hereinafter Clukey.
3. Regarding claim 1, Clukey discloses (Fig 3) an electrostatic discharge protection device (10; col 4 ln 59-60) comprising:
 - a first bipolar transistor (Q3; col 4 ln 62) and a second bipolar transistor (Q2; col 4 ln 61) coupled in series (apparent in Fig 3: series is I/O Pin-40-C-30-GND), and
 - an emitter (40) of the first bipolar transistor being coupled (col 5 ln 9-10) to a protected node (I/O Pin) and an emitter (30) of the second bipolar transistor being coupled (col 5 ln 8-9) to a grounded node (GND), the first bipolar transistor and the second bipolar transistor having a common collector (C; col 4 ln 62).
4. Regarding claim 2, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 1, the first bipolar transistor (Q3) and the second bipolar transistor (Q2) being npn transistors (col 5 ln 42-50, 55-58).

Art Unit: 2811

5. Regarding claim 7, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 2, the common collector being formed by a first n-type region (12; col 5 In 36-37, 55-58).

6. Regarding claim 8, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 2, the first n-type region being coupled to a first p-type region (41; col 5 In 46-47, 55-58) and a second p-type region (31; col 5 In 46-47, 55-58), the first p-type region forming a base of the first bipolar transistor (col 5 In 46-47, 55-58), the second p-type region forming a base of the second bipolar transistor (col 5 In 46-47, 55-58).

7. Regarding claim 9, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 8, comprising an n-type doped isolation region (15; col 5 In 42-43) that substantially surrounds and separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of 15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

8. Regarding claim 10, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 9, comprising a second n-type region (40; col 5 In 49-50, 55-58) and a third n-type region (30; col 5 In 49-50, 55-58), the second n-type region being formed within the first p-type region (40 is clearly within 41; col 5 In 49-51) and separated from the first n-type region (40 is clearly separated from 12), the third n-type region being formed within the second p-type region (30 is clearly within 31; col 5 In 49-

Art Unit: 2811

51) and separated from the first n-type (30 is clearly separated from 12), the second n-type region (40) forming the emitter (col 5 ln 49; ln 10) of the first bipolar transistor (Q3) and the third n-type region (30) forming the emitter (col 5 ln 49; ln 8) of the second bipolar transistor (Q2).

9. Regarding claim 11, Clukey discloses (Fig 4) an electrostatic discharge protection device (10; col 5 ln 34) comprising:

a p-type semiconductor substrate (11; col 5 ln 34-35, 55-58);

an n-type buried layer (12; col 5 ln 36-37, 55-58) provided in the p-type semiconductor substrate (clearly 12 is in 11; col 5 ln 34-36);

a first p-type region (41; col 5 ln 46-47, 55-58) and a second p-type region (31; col 5 ln 46-47, 55-58) overlying the n-type buried layer (41 and 31 clearly overly 12), the first p-type region and the second p-type region being separated from one another (41 and 31 are clearly separated; col 5 ln 40-42);

a first n+ type region (40; col 5 ln 49-50, 55-58) provided in the first p-type region (40 is clearly in 41; col 5 ln 49-51);

a second n+ type region (30; col 5 ln 49-50, 55-58) provided in the second p-type region (30 is clearly in 31; col 5 ln 49-51); and

the first n+ type region, the first p-type region, and the n-type buried layer forming a first bipolar npn transistor (Q3; col 5 ln 9-10, 36, 46-47, 55-58), the second n+ type region, the second p-type region, and the n-type buried layer forming a second bipolar npn transistor (Q2; col 5 ln 8, 36, 45, 55-58), the first bipolar npn transistor and the second bipolar npn transistor including a common collector (12; col 5 ln 36).

Further regarding claim 11, the term n^+ is a relative term, and nothing in the specification or claims prevents reading this limitation onto regions 30 and 40.

10. Regarding claim 12, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 11, the first bipolar npn transistor and the second bipolar npn transistor being coupled in series (apparent in Fig 3: series is I/O Pin-40-C-30-GND).

11. Regarding claim 13, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 12, further comprising an n-well isolation region (15; col 5 ln 42-43) that separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of 15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

12. Regarding claim 14, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 11, the first n^+ type region functioning as an emitter of the first bipolar npn transistor (col 5 ln 9-10), and the second n^+ type region functioning as an emitter of the second bipolar npn transistor (col 5 ln 8).

13. Regarding claim 15, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 14, the first p-type region functioning as a base region (col 5 ln 46-47) of the first bipolar npn transistor (41 is clearly part of Q3), and the second p-type region functioning as a base region (col 5 ln 46) of the second bipolar npn transistor (31 is clearly part of Q2).

Art Unit: 2811

14. Regarding claim 16, Clukey discloses (Fig 4) the electrostatic discharge protection device of claim 15, the n-type buried layer functioning as a common collector for both the first bipolar npn transistor and the second bipolar npn transistor (col 5 ln 36).

15. Regarding claim 18, Clukey inherently discloses a method for fabrication of an ESD protection device (Clukey discloses the structure, which, inherently, must have been formed by providing the structure), the method comprising:

providing an n-type buried layer (12; col 5 ln 36-37, 55-58) in a p-type semiconductor substrate (11; col 5 ln 34-35, 55-58);

forming a first p-type region (41; col 5 ln 46-47, 55-58) and a second p-type region (31; col 5 ln 46-47, 55-58) overlying the n-type buried layer (41 and 31 clearly overly 12), the first p-type region and the second p-type region being separated from one another (41 and 31 are clearly separated; col 5 ln 40-42);

forming a first n+ type region (40; col 5 ln 49-50, 55-58) in the first p-type region (40 is clearly in 41; col 5 ln 49-51);

forming a second n+ type region (30; col 5 ln 49-50, 55-58) in the second p-type region (30 is clearly in 31; col 5 ln 49-51); the first n+ type region, the first p-type region, and the n-type buried layer defining a first bipolar npn transistor (Q3; col 5 ln 9-10, 36, 46-47, 55-58), the second n+ type region, the second p-type region, and the n-type buried layer defining a second bipolar npn transistor (Q2; col 5 ln 8, 36, 45, 55-58).

Further regarding claim 18, the term n+ is a relative term, and nothing in the specification or claims prevents reading this limitation onto regions 30 and 40.

Art Unit: 2811

16. Regarding claim 19, Clukey inherently discloses (Fig 4) the method of claim 18, further comprising (Clukey discloses the structure, which, inherently, must have been formed) forming an n-well isolation region (15; col 5 ln 42-43) that separates the first p-type region and the second p-type region. The term isolation region has been broadly interpreted to include any region that can separate regions from one another. Although the portions of regions 15 underlying the p-type base regions 31 and 41 serve as collector regions, the portions of 15 laterally adjacent to the p-type base regions 31 and 41 separate the p-type base regions 31 and 41.

17. Regarding claim 20, Clukey discloses the method of claim 19, the first n+ type region functioning as an emitter of the first bipolar npn transistor (col 5 ln 9-10), and the second n+ type region functioning as an emitter of the second bipolar npn transistor (col 5 ln 8), the first p-type region functioning as a base region (col 5 ln 46-47) of the first bipolar npn transistor (41 is clearly part of Q3), the second p-type region functioning as a base region (col 5 ln 46) of the second bipolar npn transistor (31 is clearly part of Q2), and the n-type buried layer functioning as a collector for both the first bipolar npn transistor and the second bipolar npn transistor (col 5 ln 36).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 3-5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clukey in view of Vashchenko et al. (US 6,560,081), hereinafter Vashchenko.

20. Regarding claim 3, Clukey discloses the electrostatic discharge protection device of claim 1, but does not disclose further comprising a clamp electrically coupled between the protected node and a base of the second bipolar transistor. Vashchenko is analogous art, which discloses (Fig 2) a clamp (104; col 3 ln 5-6) electrically coupled between a protected node (102; col 3 ln 1-2) and a base (116; col 3 ln 13-14, 18-19) of a bipolar transistor (114; col 3 ln 13-14).

21. Further regarding claim 3, the field of endeavor is electrostatic discharge protection devices utilizing bipolar transistors coupled between a protected node and a ground node, for both Clukey (col 4 ln 59-62; Fig 3) and Vashchenko (col 3 ln 13-15, col 4 ln 16-17, Fig 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Clukey by providing the clamp (104) of Vashchenko between the protected node (Clukey I/O Pin) and the base of the bipolar transistor whose emitter is connected to ground (Clukey Q2); for at least the purpose of fast switching of the bipolar transistor (Vashchenko col 3 ln 47-49).

22. Regarding claim 4, Vashchenko discloses the clamp comprising a two-terminal circuit (110 and 112; col 3 ln 5-9).

23. Regarding claim 5, Vashchenko discloses the two-terminal circuit being configured to breakdown before the bipolar transistor (col 3 ln 41-44) to reduce the overall trigger voltage of the electrostatic discharge protection device (col 3 ln 44-47).

Art Unit: 2811

24. Regarding claim 17, Clukey discloses the electrostatic discharge protection device of claim 16, but does not disclose further comprising a two-terminal circuit electrically coupled between the protected node and a base of the second bipolar transistor, the two-terminal circuit being configured to breakdown before the first and second bipolar transistor break down to reduce the overall trigger voltage of the electrostatic discharge protection device. Vashchenko is analogous art which discloses (Fig 2) a clamp (104; col 3 ln 5-6) electrically coupled between a protected node (102; col 3 ln 1-2) and a base (116; col 3 ln 13-14, 18-19) of a bipolar transistor (114; col 3 ln 13-14) , the two-terminal circuit being configured to breakdown before the bipolar transistor (col 3 ln 41-44) to reduce the overall trigger voltage of the electrostatic discharge protection device (col 3 ln 44-47).

25. Further regarding claim 17, the field of endeavor is electrostatic discharge protection devices utilizing bipolar transistors coupled between a protected node and a ground node, for both Clukey (col 4 ln 59-62; Fig 3) and Vashchenko (col 3 ln 13-15, col 4 ln 16-17, Fig 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Clukey by providing the clamp (104) of Vashchenko between the protected node (Clukey I/O Pin) and the base of the bipolar transistor whose emitter is connected to ground (Clukey Q2); for at least the purpose of fast switching of the bipolar transistor (Vashchenko col 3 ln 47-49).

26. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clukey in view of Vashchenko as applied to claim 4 above, and further in view of Mallikarjunaswamy et al (US 6,888,710) – hereinafter Mallikarjunaswamy.

27. Regarding claim 6, the combined device of Clukey and Vashchenko differs from the claimed invention only in not disclosing the two-terminal circuit comprising “an NMOS transistor.” Mallikarjunaswamy discloses an analogous ESD protection device and teaches the use of a clamp comprising a two-terminal circuit comprising an NMOS transistor (col 3 ln 39-41). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Clukey by providing a clamp electrically coupled between the protected node and a base of the second bipolar transistor, the clamp comprising a two-terminal circuit, the two-terminal circuit comprising an NMOS transistor, as taught by Mallikarjunaswamy; at least to dissipate charge from the protected node almost instantly (Mallikarjunaswamy: col 3 ln 60-62).

28. Further regarding claim 6, modification to Clukey (as applied to claim 3) has been described in view of Mallikarjunaswamy only, since applicant’s amendment to claim 6 does not strictly require the modification to Clukey in view of Vashchenko.

Response to Arguments

29. Applicant’s arguments filed 11/14/2005 with respect to claims 1-5 and 7-20 have been fully considered but they are not persuasive.

30. Applicant’s arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

31. Examiner concurs with applicant's observation that "Independent claim 1 (and 11) positively recites an electrostatic discharge protection device having a first bipolar transistor and a second bipolar transistor." Examiner does not concur with applicant's argument that "These advantageously claimed features are not taught or suggested by the patents granted to Clukey and Vashchenko et al.; either alone or in combination." Clukey discloses (Fig 3) an electrostatic discharge protection device (10; col 4 ln 59-60) comprising: a first bipolar transistor (Q3; col 4 ln 62) and a second bipolar transistor (Q2; col 4 ln 61).

32. Regarding applicant's arguments that "Clukey teaches away from the advantageously claimed invention because Clukey teaches that a third transistor is required" and that "Applicants advantageously claimed invention is distinct from - and superior to - the device taught by Clukey", examiner notes that applicant's claim language ("comprising"; claim 1 line 1) is open-ended. Clukey adds to, but does not teach away from, applicant's invention as claimed; which is not distinct from Clukey, since "comprising" allows for additional elements.

33. Examiner concurs with applicant's observation that "element 15 is part of the common collector." However, examiner maintains the rejection of claim 9. Clukey discloses (Fig 4) base regions 31 and 41 are isolated from one another by, *inter alia*, upper portions of 15. Examiner does not concur with applicant's argument that "Clukey does not teach that either the common collector element 15 or the isolation elements 14/16 and 14'/16' substantially surround the first p-type region and the second p-type

region as advantageously claimed.” Clukey discloses (Fig 4) that first p-type region (41) and second p-type region (31) are surrounded by 14, 15, and 16.

34. Examiner concurs with applicant’s observation that “Vashchenko et al. does not teach or suggest a first bipolar transistor and a second bipolar transistor having a common collector as advantageously claimed” but finds this argument moot, since Vashchenko has not been relied upon to teach these elements.

35. Examiner concurs with applicant’s observations that “a three transistor structure has a very different electrical operation than a single transistor structure” and that “Clukey states that the single transistor structure...is problematic.” However, as is known to students of introductory electrical engineering, operating principles of one, often simple, circuit are frequently used to advantageously modify other, often larger, circuits. Examiner does not concur with applicant’s argument that “it would not be obvious to one of ordinal skill in the art to add a portion of the Vashchenko et al. circuit to the Clukey circuit. The field of endeavor is electrostatic discharge protection devices utilizing bipolar transistors coupled between a protected node and a ground node, for both Clukey (col 4 ln 59-62; Fig 3) and Vashchenko (col 3 ln 13-15, col 4 ln 16-17, Fig 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Clukey by providing the clamp (104) of Vashchenko between the protected node (Clukey I/O Pin) and the base of the bipolar transistor whose emitter is connected to ground (Clukey Q2); for at least the purpose of fast switching of the bipolar transistor (Vashchenko col 3 ln 47-49).

Conclusion

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

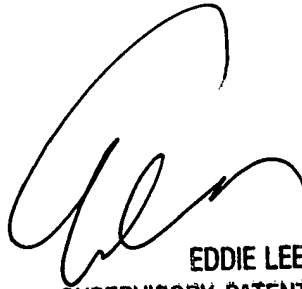
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800